ABSTRACT

[1078] An MN counter with analog interpolation (an "MNA counter") includes an MN counter, a multiplier, a delay generator, and a current generator. The MN counter receives an input clock signal and M and N values, accumulates M for each input clock cycle using a modulo-N accumulator, and provides an accumulator value and a counter signal with the desired frequency. The multiplier multiplies the accumulator value with an inverse of M and provides an L-bit control signal. The current generator implements a current locked loop that provides a reference current for the delay generator. The delay generator is implemented with a differential design, receives the counter signal and the L-bit control signal, compares a differential signal generated based on the counter and control signals, and provides the output clock signal. The leading edges of the output clock signal have variable delay determined by the L-bit control signal and the reference current.